## AMENDMENTS TO THE CLAIMS

Please **CANCEL** claim 26 without prejudice or disclaimer.

Please **AMEND** claims 24, 25, 27-32 and 34-36 as shown below.

The following is a complete list of all claims in this application.

1-23. (Canceled)

24. (Currently Amended) A method for fabricating a thin film transistor array substrate having a display area and a peripheral area ~~for a liquid crystal display~~, comprising ~~the~~ steps of:

forming a gate line assembly and a common electrode line assembly on a substrate ~~including a display areas and a peripheral areas~~, the gate line assembly comprising a plurality of gate lines, ~~and~~ a plurality of gate ~~electrode~~ electrodes ~~of the display areas,~~ and a plurality of gate pads ~~of the peripheral areas~~, the common electrode line assembly comprising a plurality of common signal lines and a plurality of common electrodes, the gate pads being arranged in the peripheral area ~~of the display areas~~;

placing a shadow frame over the substrate, the shadow frame comprising a first deposition blocking area covering the gate pads;

forming a gate insulating layer covering the gate line assembly and exposing the portions of the gate pads;

forming a semiconductor layer ~~pattern~~;

forming an ohmic contact layer ~~pattern~~; ~~and~~

forming a data line ~~assembly~~ layer;

forming a conductive layer; and

simultaneously patterning the semiconductor layer, the ohmic contact layer, the data line layer and the conductive layer to form a semiconductor pattern, an ohmic contact pattern, a data line assembly and a plurality of pixel electrodes, respectively, ~~and pixel electrodes~~, the data line assembly comprising a plurality of data lines, a plurality of source electrodes, ~~and~~ a plurality of drain electrodes ~~of the display areas,~~ and a plurality of data pads ~~of the peripheral areas~~, the data pads being arranged in the peripheral area, ~~the pixel electrodes being electrically connected to the drain electrodes while proceeding parallel to the common electrodes;~~

wherein the step of simultaneously patterning is performed by using a single photoresist pattern comprising:

a first portion placed between the source electrode and the drain electrode having a first thickness;

a second portion for forming the data line assembly and the pixel electrodes and having a second thickness greater than the first thickness; and

a third portion having a third thickness smaller than the first portion.

~~a shadow frame having a first deposition blocking areais used to prevent the gate insulating layer from being deposited on the gate pads of the peripheral areas in the step of forming the gate insulating layer.~~

25. (Currently Amended) The method of claim 24, wherein the shadow frame ~~has~~ further comprises a second deposition blocking area covering the data pads ~~areato prevent the gate insulating layer, the semiconductor pattern, or the ohmic contact pattern from being deposited on areas for the data pads of the peripheral areas~~.

26. (Cancelled).

27. (Currently Amended) The method of claim ~~26~~ 24, wherein the step of simultaneously patterning is performed by using a single mask ~~the data line assembly, the ohmic contact pattern and the semiconductor pattern are formed through a photolithography using one mask~~.

28. (Currently Amended) The method of claim 27, wherein the step of simultaneously patterning comprises steps of: ~~steps of forming the gate insulating layer, the semiconductor pattern, the ohmic contact layer pattern, and the data line assembly comprise:~~

~~depositing the gate insulating layer, a semiconductor layer, an ohmic contact layer, and a conductor layer:~~

coating a photoresist layer on the ~~conductor~~ conductive layer;

exposing the photoresist layer to light through the mask;

~~forming the photoresist pattern such that the second portion lies on the data line assembly~~ ~~by~~ developing the photoresist layer to form the photoresist pattern; and

~~forming the data line assembly, the ohmic contact layer pattern, and the semiconductor pattern respectively made of the conductor layer, the ohmic contact layer and the semiconductor layer by removing a portion of the conductor layer under the third portion, the semiconductor layer and the ohmic contact layer thereunder, the first portion, the conductor layer and the ohmic contact layer under the first portion, and a partial thickness of the second portion; and~~

etching the semiconductor layer, the ohmic contact layer, the data line layer and the conductive layer; and

removing the photoresist pattern.

29. (Currently Amended) The method of claim 28, wherein the step of etching comprises steps of: ~~forming the data wire, the ohmic contact layer pattern and the semiconductor pattern comprises;~~

etching ~~removing the portion~~ portions of the ~~conductor~~ conductive layer under the third portion ~~by dry or wet etching~~ to expose the ohmic contact layer;

~~dry~~ etching portions of the ohmic contact layer and ~~under the third portion,~~ the semiconductor layer ~~thereunder~~ covered by the third portion and the first portion to ~~obtain~~ form the ~~completed~~ semiconductor pattern ~~along with exposing~~ and to expose the gate insulating layer ~~under~~ covered by the third portion and the ~~conductor~~ conductive layer ~~under~~ covered the first portion; and

removing portions of the ~~conductor~~ conductive layer and the ohmic contact layer covered by ~~under~~ the first portion ~~and the ohmic contact layer thereunder~~ to ~~complete~~ form the data wire pattern and the ohmic contact ~~layer~~ pattern.

30. (Currently Amended) The method of claim 29, wherein the shadow frame prevents ~~is used to prevent~~ the semiconductor layer, the ohmic contact layer, or the ~~conductor~~ conductive layer from being deposited on the gate pads ~~pad of the peripheral areas in the step of depositing the semiconductor layer, the ohmic contact layer, and the conductor layer~~.

31. (Currently Amended) The method of claim 30, wherein the photoresist pattern ~~has~~ further comprises a fourth portion placed on the gate pad portions~~,~~ and having a thickness substantially the same with one of ~~the thickness of~~ the first portion, the second portion~~,~~ or the third portion.

32. (Currently Amended) The method of claim 28 ~~26~~, wherein the photoresist layer is formed of a positive photoresist material, and

the ~~a~~ mask comprises: ~~used for forming the photoresist pattern has~~

a first~~,~~ part having a first transmittance and exposing the first portion of the photoresist pattern;

a second~~,~~ part having a second transmittance smaller than the first transmittance and exposing the second portion of the photoresist pattern; and

a third part~~,~~ having a third transmittance greater than the first transmittance and exposing the third portion of the photoresist pattern.

~~the transmittance of the third part is higher than the first and the second parts, the transmittance of the first part is higher than the second part, the photoresist pattern is made of a positive photoresist, and~~

~~the mask is aligned such that the first, the second, and the third parts respectively face the first, the second, and the third portions of the photoresist pattern in an exposing step.~~

33. (Original) The method of claim 32, wherein the first part of the mask includes a partially transparent layer.

34. (Currently Amended) The method of claim 32, the first part of the mask includes a plurality of slit patterns smaller than the resolution of ~~the~~ an exposure device used in the exposing step.

35. (Currently Amended) The method of claim 24 ~~26~~, wherein the first portion is formed by reflow.

36. (Currently Amended) The method of claim 24, further comprising ~~the~~ a step of depositing a passivation layer~~;~~, wherein the shadow frame ~~is used to prevent~~ prevents the passivation layer from being deposited on t~~he peripheral areas having~~ the gate pads and the data pads.